COLUMBIA UNIVERSITY
IN THE CITY OF NEW YORK

Columbia Integrated Systems Laboratory

MOSIS

DIGITAL CLOCK TESTING REPORT

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VLSI DESIGN LAB(ELEN 6350)
SPRING 2016 – Prof. Peter Kinget

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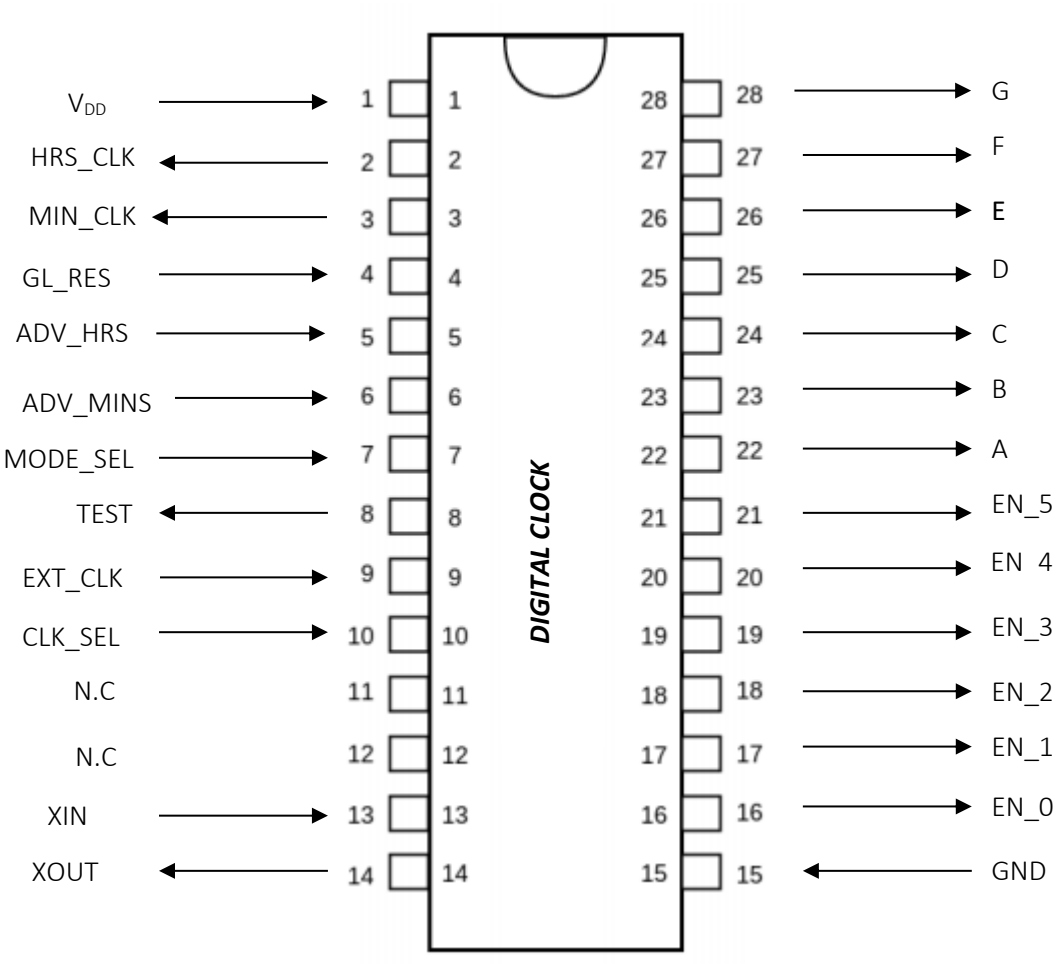
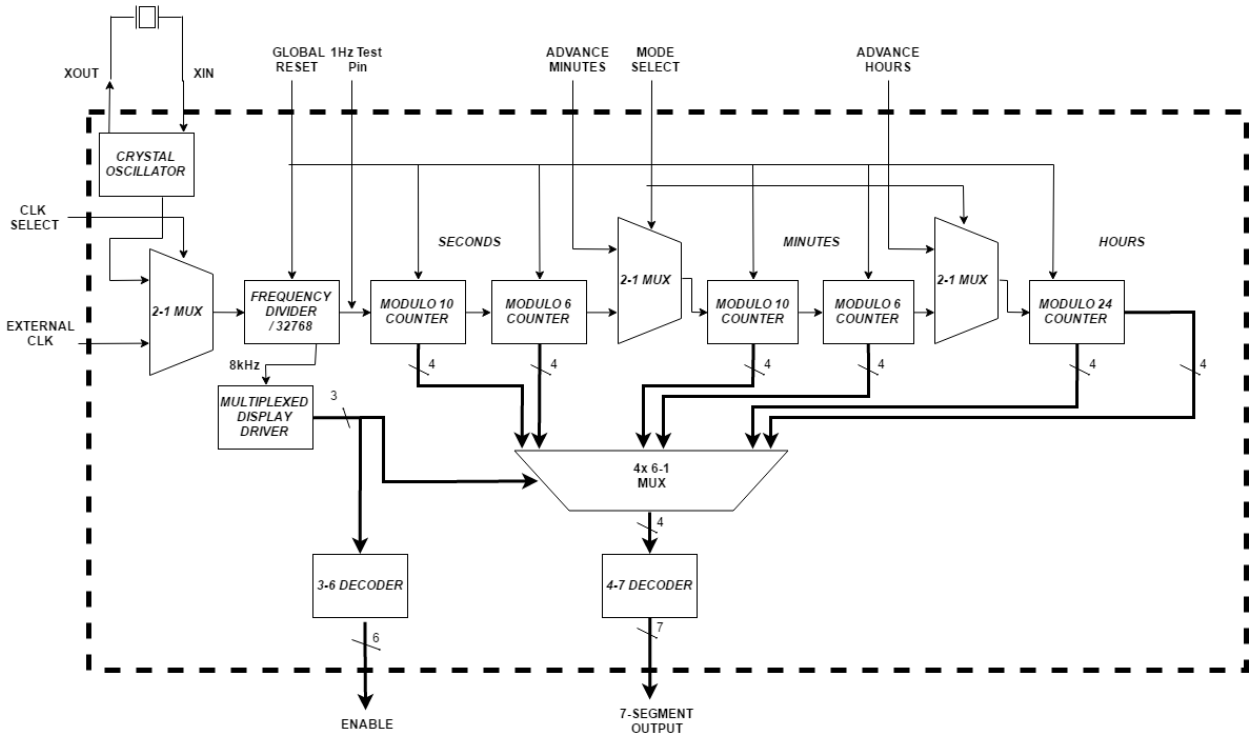
1. Pin Diagram

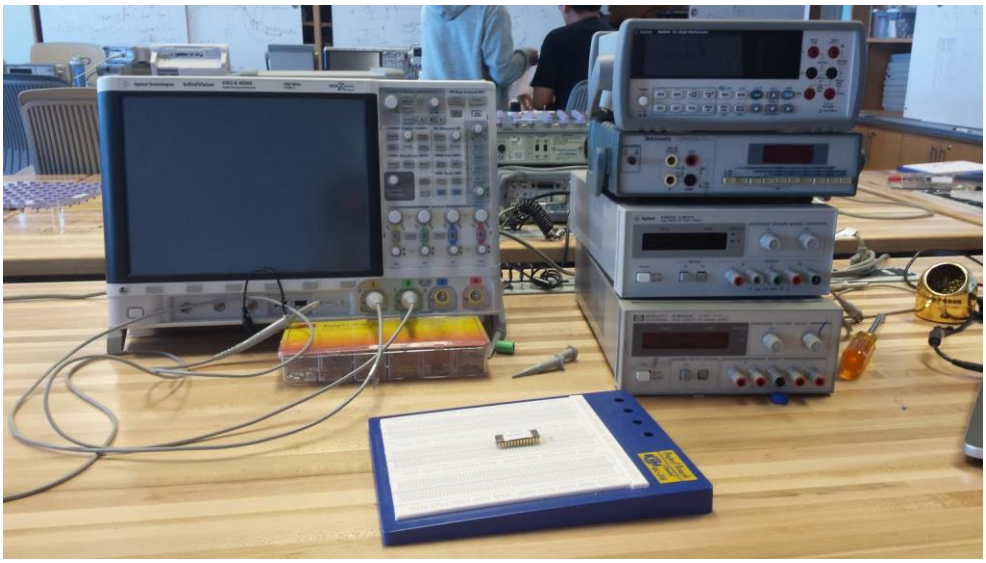


2. Block Diagram



* Dotted line represents chip boundary.

3. Testing



For the testing we will use V_{DD} = 1.2V as Power Supply, a Frequency Generator indicated as FG, an Oscilloscope indicated as Osc-CH# where CH# is the channel number and finally N.C. as No Connection.

3.1 Power Supply to the chip

Before proceeding we first need to power up the chip and check for Power to Ground sorting:

We notice that no current is flowing between Power and Ground so we can proceed.

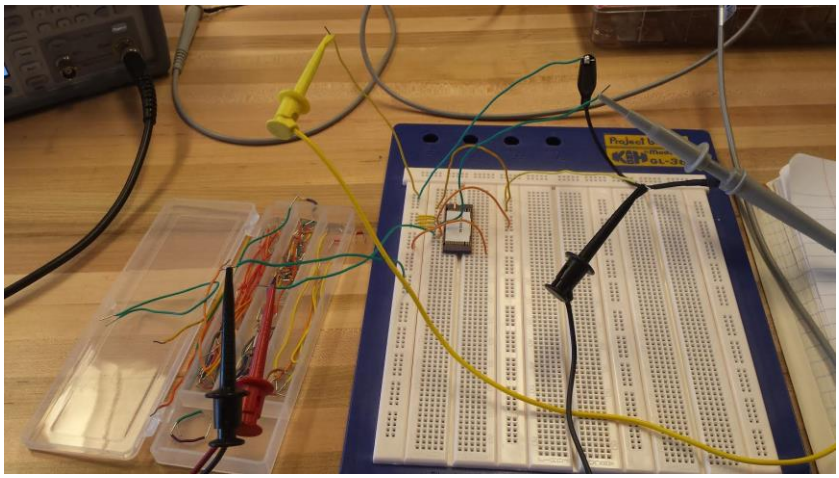
3.2 1Hz Test Pin

The first step for testing our chip is verifying the 1Hz frequency at the output of the frequency division chain comprised of 15 2-divider DFF's. In order to obtain desirable HHIGH and LOW voltage values, We will set the frequency generator as:

- Waveform Type: Square Wave
- Frequency: 32.768kHz
- Amplitude: $1.2V_{pp}$
- Offset: 0.6V
- Duty Cycle: 50%
- Output: High-Z

The pin connections must be:

Pin#	Pin Name	Connection	Pin#	Pin Name	Connection
1	V_{DD}	V_{DD}	15	GND	GND
2	HRS_CLK	N.C.	16	EN_0	N.C.
3	MIN_CLK	N.C.	17	EN_1	N.C.
4	GL_RES	GND	18	EN_2	N.C.
5	ADV_HRS	GND	19	EN_3	N.C.
6	ADV_MIN	GND	20	EN_4	N.C.
7	MODE_SEL	GND	21	EN_5	N.C.
8	1Hz_TEST	Osc-CH1	22	A	N.C.
9	EXT_CLK	F.G.	23	B	N.C.
10	CLK_SEL	V_{DD}	24	C	N.C.
11	N.C.	N.C	25	D	N.C.
12	N.C.	N.C.	26	E	N.C.
13	XIN	N.C	27	F	N.C.
14	XOUT	N.C	28	G	N.C.



Below we can see the 1Hz Output of the 1Hz_TEST pin in the Oscilloscope.

3.3 Minutes MSD MSB

The next output we will test is the MIN_CLK pin. This the inverted output is the MSB of the MSD of the Seconds:

16:45:23

↓

010

↓

(MIN_CLK)’

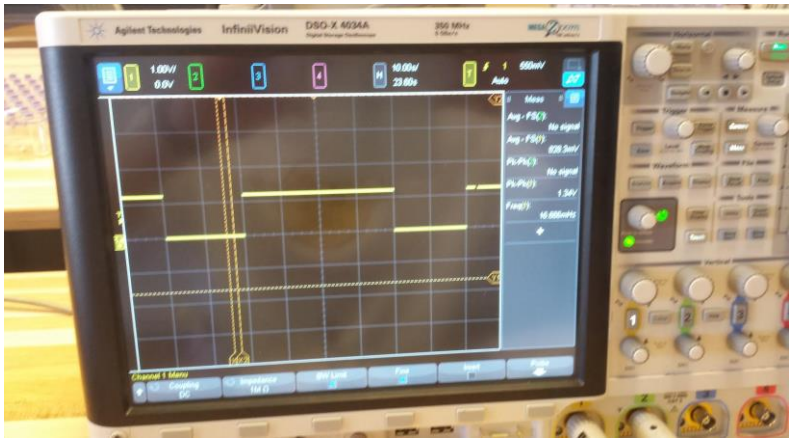
This pin is asserts and de-asserts once every 60s. More specifically the truth table of the MSD is:

SECONDS MSD			SECONDS	MIN_CLK
0	0	0	0-10	**1**
0	0	1	10-20	**1**
0	1	0	20-30	**1**
0	1	1	30-40	**1**
1	0	0	40-50	**0**
1	0	1	50-60	**0**

The Pin configuration is as follows:

Pin#	Pin Name	Connection	Pin#	Pin Name	Connection
1	V_{DD}	V_{DD}	15	GND	GND
2	HRS_CLK	N.C.	16	EN_0	N.C.
3	MIN_CLK	Osc-CH1	17	EN_1	N.C.
4	GL_RES	GND	18	EN_2	N.C.
5	ADV_HRS	GND	19	EN_3	N.C.
6	ADV_MIN	GND	20	EN_4	N.C.
7	MODE_SEL	GND	21	EN_5	N.C.
8	1Hz_TEST	N.C.	22	A	N.C.
9	EXT_CLK	F.G.	23	B	N.C.
10	CLK_SEL	V_{DD}	24	C	N.C.
11	N.C.	N.C	25	D	N.C.
12	N.C.	N.C.	26	E	N.C.
13	XIN	N.C	27	F	N.C.
14	XOUT	N.C	28	G	N.C.

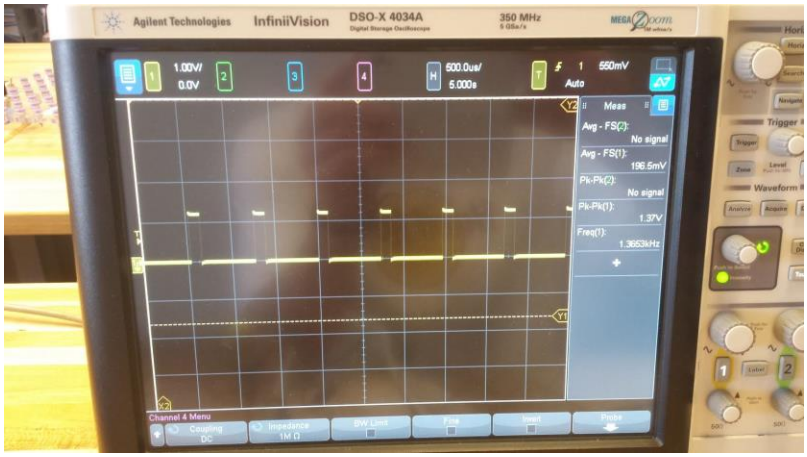
The result can be seen in the Oscilloscope:



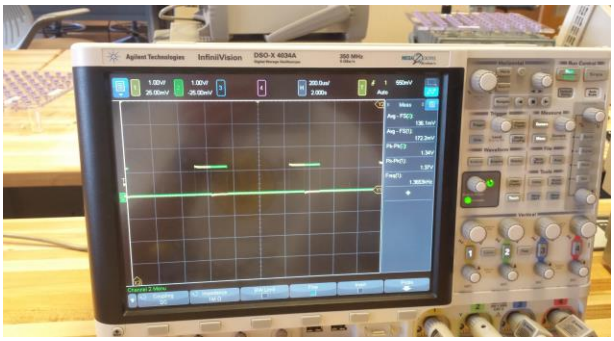
3.4 Enable Signals

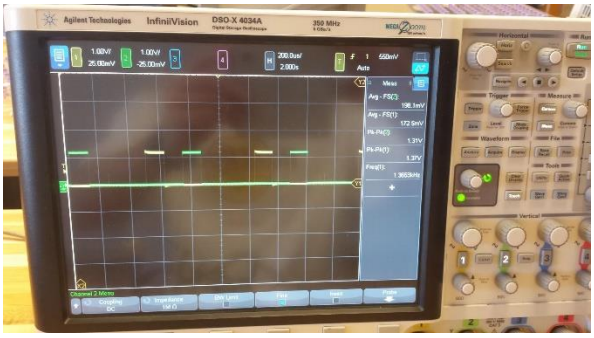
In order to view the EN_5 signal that concerns the LSD of the seconds the connections must be as follows:

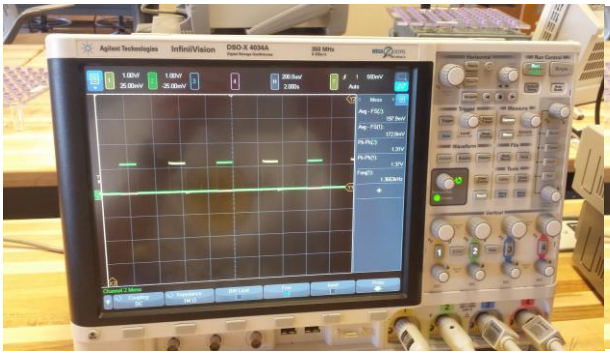
Pin#	Pin Name	Connection	Pin#	Pin Name	Connection
1	V_{DD}	V_{DD}	15	GND	GND
2	HRS_CLK	N.C.	16	EN_0	N.C.
3	MIN_CLK	N.C.	17	EN_1	N.C.
4	GL_RES	GND	18	EN_2	N.C.
5	ADV_HRS	GND	19	EN_3	N.C.
6	ADV_MIN	GND	20	EN_4	N.C.
7	MODE_SEL	GND	21	EN_5	Osc-CH1
8	1Hz_TEST	N.C.	22	A	N.C.
9	EXT_CLK	F.G.	23	B	N.C.
10	CLK_SEL	V_{DD}	24	C	N.C.
11	N.C.	N.C	25	D	N.C.
12	N.C.	N.C.	26	E	N.C.
13	XIN	N.C	27	F	N.C.
14	XOUT	N.C	28	G	N.C.

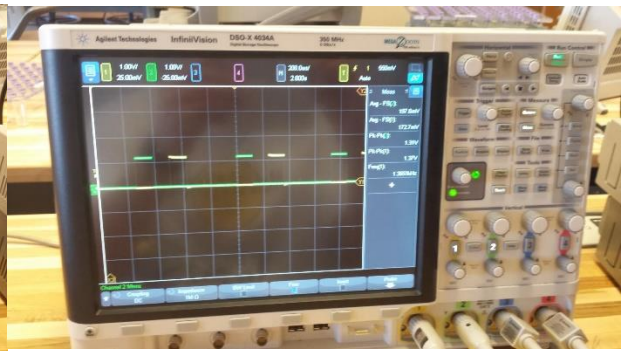


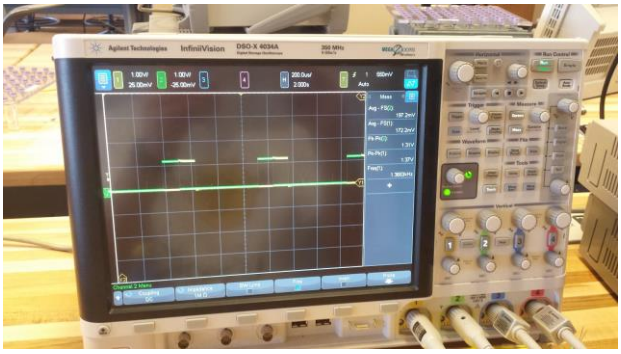
Now, to verify that every enable signal is adjacent to the previews and the next we have to keep the oscilloscope channel 1 at EN_5 and channel 2 at EN_4, EN_3, EN_2, EN_1, EN_0 sequentially.











3.5 7-Segment LED Display Verification

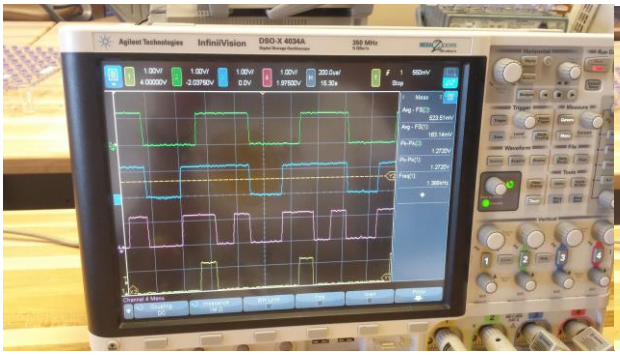
To verify the 7-segmens LED Display we will check the LSD of the seconds, which means outputting EN_5 and simultaneously look at the E,F,G segments for 10s and check if they satisfy the truth table below:

Binary Inputs	Decoder Outputs	7 Segment Display Outputs
D C B A	a b c d e f g	
0 0 0 0	1 1 1 1 1 1 0	0
0 0 0 1	0 1 1 0 0 0 0	1
0 0 1 0	1 1 0 1 1 0 1	2
0 0 1 1	1 1 1 1 0 0 1	3
0 1 0 0	0 1 1 0 0 1 1	4
0 1 0 1	1 0 1 1 0 1 1	5
0 1 1 0	1 0 1 1 1 1 1	6
0 1 1 1	1 1 1 0 0 0 0	7
1 0 0 0	1 1 1 1 1 1 1	8
1 0 0 1	1 1 1 1 0 1 1	9

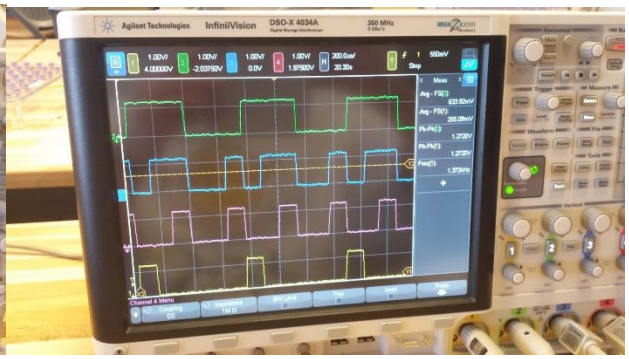
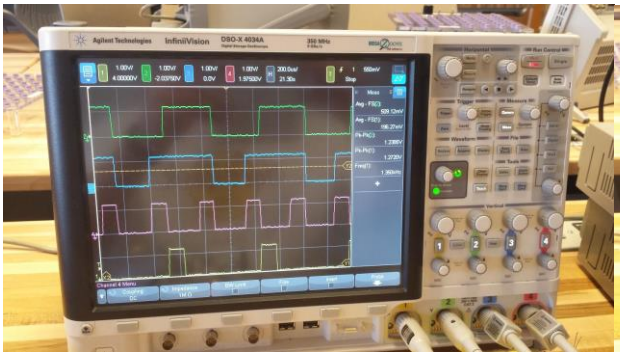
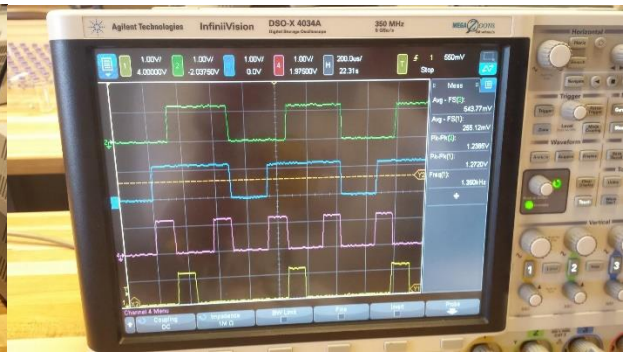
The pin connections are shown below:

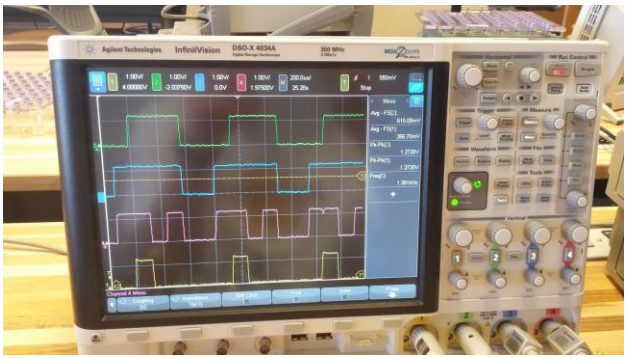
Pin#	Pin Name	Connection	Pin#	Pin Name	Connection
1	V_{DD}	V_{DD}	15	GND	GND
2	HRS_CLK	N.C.	16	EN_0	N.C.
3	MIN_CLK	N.C.	17	EN_1	N.C.
4	GL_RES	GND	18	EN_2	N.C.
5	ADV_HRS	GND	19	EN_3	N.C.
6	ADV_MIN	GND	20	EN_4	N.C.
7	MODE_SEL	GND	21	EN_5	Osc-CH1
8	1Hz_TEST	N.C.	22	A	N.C.
9	EXT_CLK	F.G.	23	B	N.C.
10	CLK_SEL	V_{DD}	24	C	N.C.
11	N.C.	N.C	25	D	N.C.
12	N.C.	N.C.	26	E	Osc-CH2
13	XIN	N.C	27	F	Osc-CH3
14	XOUT	N.C	28	G	Osc-CH4

A 10 second run of the clock gave the outputs below:







3.6 Global Reset Verification

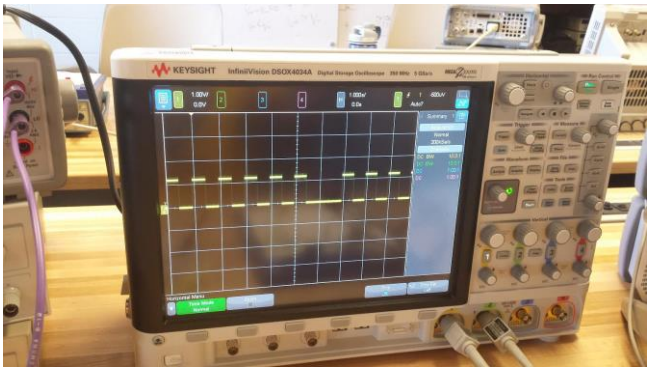
To verify the GL_RES function, we will use another frequency generator(F.G.-2) and give a 0.1Hz pulse as input to the GL_RES:

- Waveform Type: Pulse
- Frequency: 0.1Hz
- Amplitude: 1.2V_{pp}
- Offset: 0.6V
- Delay: 1s
- Output: High-Z

We need to connect the pins as shown:

Pin#	Pin Name	Connection	Pin#	Pin Name	Connection
1	V_{DD}	V_{DD}	15	GND	GND
2	HRS_CLK	N.C.	16	EN_0	N.C.
3	MIN_CLK	N.C.	17	EN_1	N.C.
4	GL_RES	F.G.-2	18	EN_2	N.C.
5	ADV_HRS	GND	19	EN_3	N.C.
6	ADV_MIN	GND	20	EN_4	N.C.
7	MODE_SEL	GND	21	EN_5	N.C.
8	1Hz_TEST	Osc-CH1	22	A	N.C.
9	EXT_CLK	F.G.-1	23	B	N.C.
10	CLK_SEL	V_{DD}	24	C	N.C.
11	N.C.	N.C	25	D	N.C.
12	N.C.	N.C.	26	E	N.C.
13	XIN	N.C	27	F	N.C.
14	XOUT	N.C	28	G	N.C.

The result on the 1Hz output is shown below:

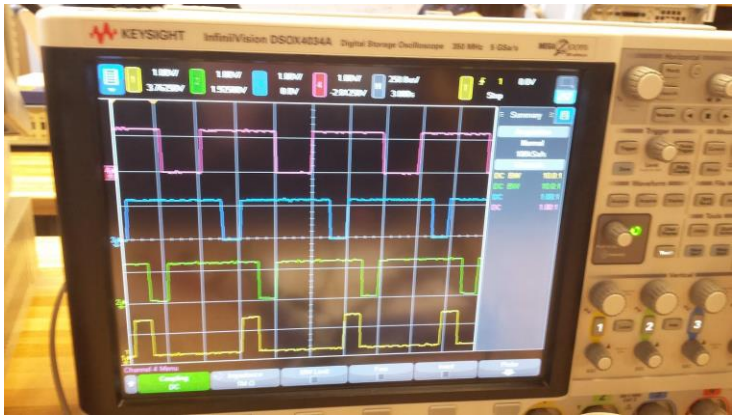


3.7 Setting Mode Verification

The setting mode will be tested by setting the MODE_SEL at the setting mode, setting a 1Hz input to the ADV_MIN and looking at EN_3 and C, D, E segments. The pin connection is shown below:

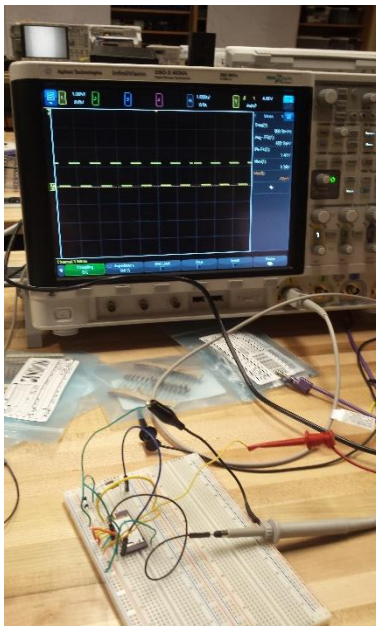
Pin#	Pin Name	Connection	Pin#	Pin Name	Connection
1	V_{DD}	V_{DD}	15	GND	GND
2	HRS_CLK	N.C.	16	EN_0	N.C.
3	MIN_CLK	N.C.	17	EN_1	N.C.
4	GL_RES	GND	18	EN_2	N.C.
5	ADV_HRS	GND	19	EN_3	Osc-CH1
6	ADV_MIN	F.G.-2	20	EN_4	N.C.
7	MODE_SEL	V_{DD}	21	EN_5	N.C.
8	1Hz_TEST	N.C	22	A	N.C.
9	EXT_CLK	F.G.-1	23	B	N.C.
10	CLK_SEL	V_{DD}	24	C	Osc-CH2
11	N.C.	N.C	25	D	Osc-CH3
12	N.C.	N.C.	26	E	Osc-CH4
13	XIN	N.C	27	F	N.C.
14	XOUT	N.C	28	G	N.C.

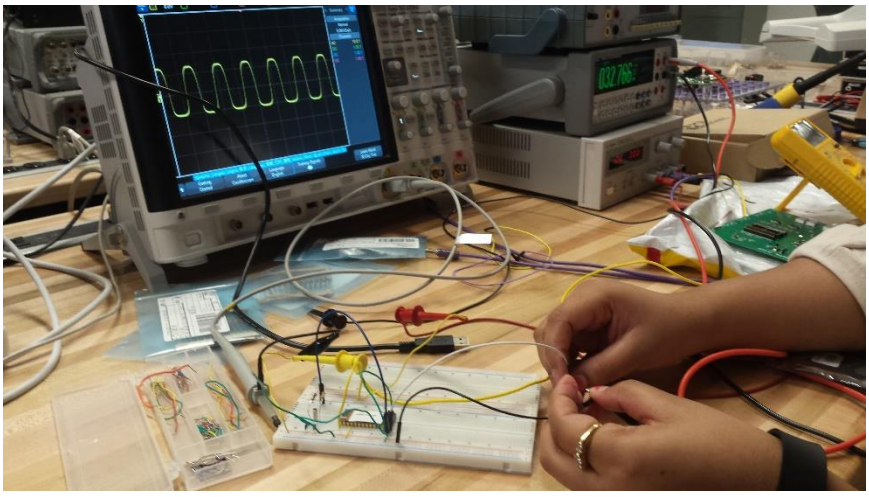
Again, we run a simulation for 10 seconds and check the C, D, E sequence to be according to the 7-segment truth table:



3.8 Crystal Oscillator Verification:

Finally, we test the crystal oscillator. We want to see the 32.768kHz frequency and 1.2 V_{pp} offset by 0.6V in the Oscillator output XIN and the 1Hz test pin having the 1Hz frequency signal:





4. PCB Testing

After verifying the chip's operation, we started testing it with the PCB:

- Power Circuitry Test

Before plugging the chip, we measured the voltage at all crucial test-points like the regulator outputs. We did it first with the 9V battery source and then with the 5V USB.

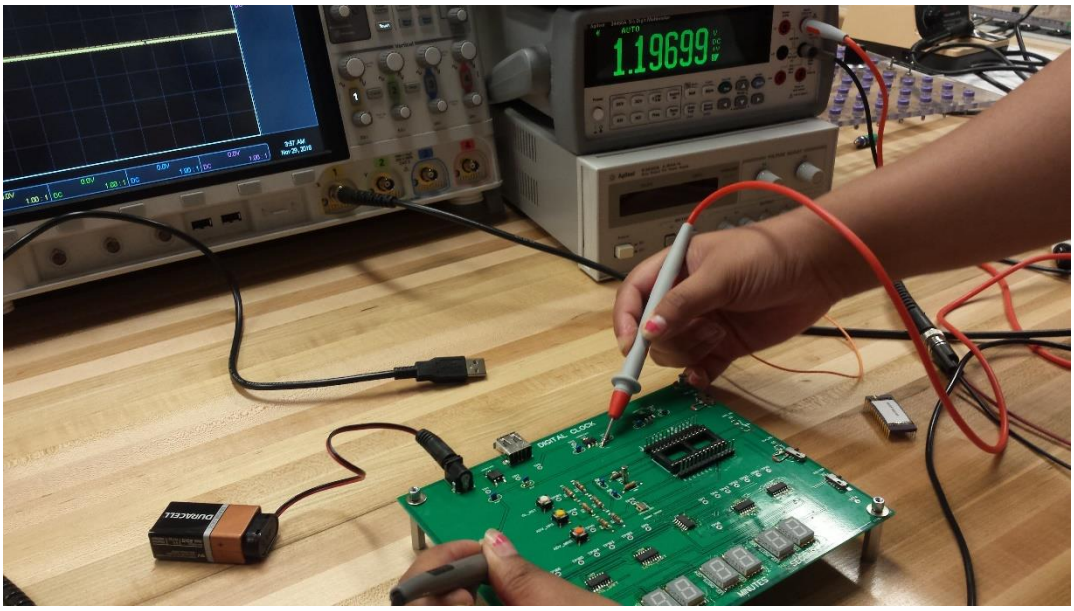


Fig. 5.4: Power Circuitry Test

- Led Display Test

Next we tested the led displays by setting proper voltage values to the A-G segments and verifying the output of the LEDs.

- External Frequency Generator Test

At this point we feel confident enough to place our chip on the PCB. Our first function test included the external frequency generator. By setting the appropriate values to our input pins, we could see the LED digits showing the proper output.

- Oscillator Test

Next we tested the crystal with the in-chip oscillator. Also we tested the external oscillator source as well.

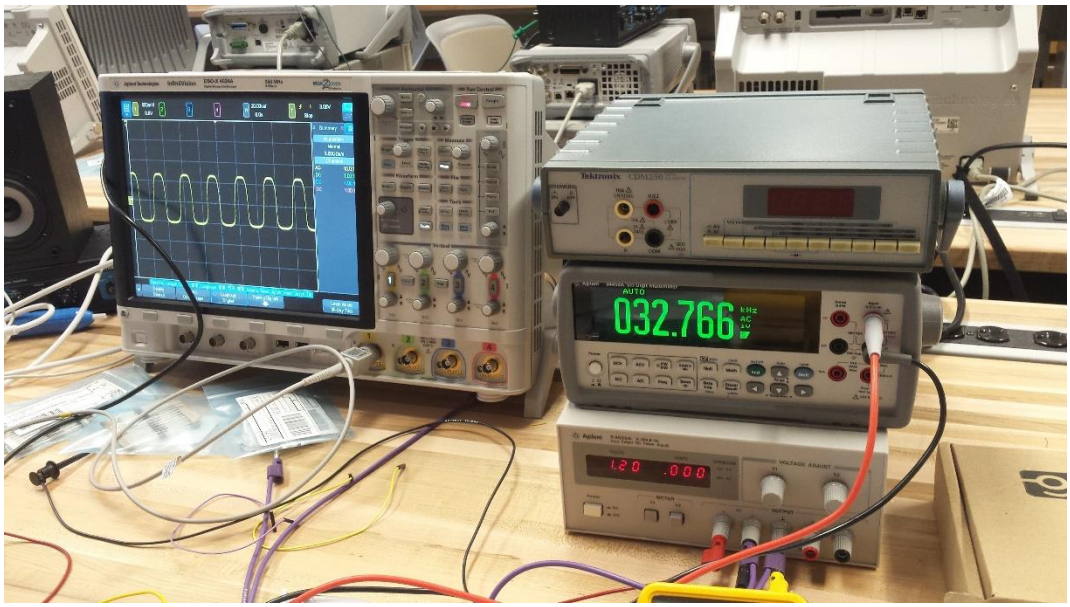


Fig. 5.5: Oscillator Test Frequency

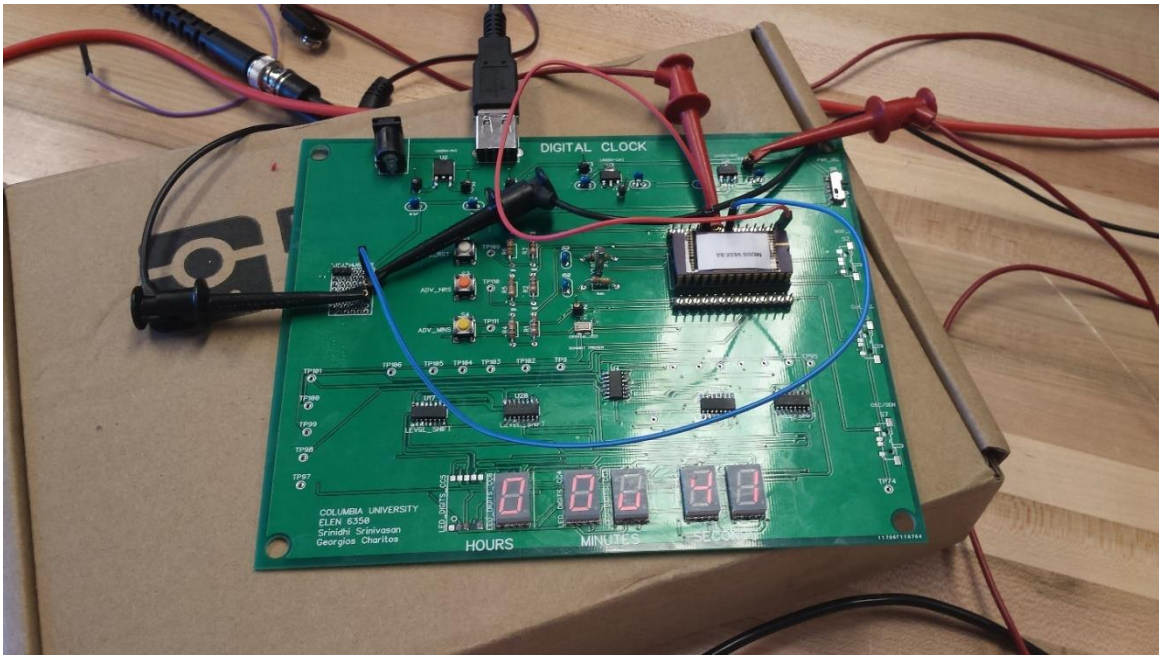


Fig. 5.6: Testing of PCB with chip mounted

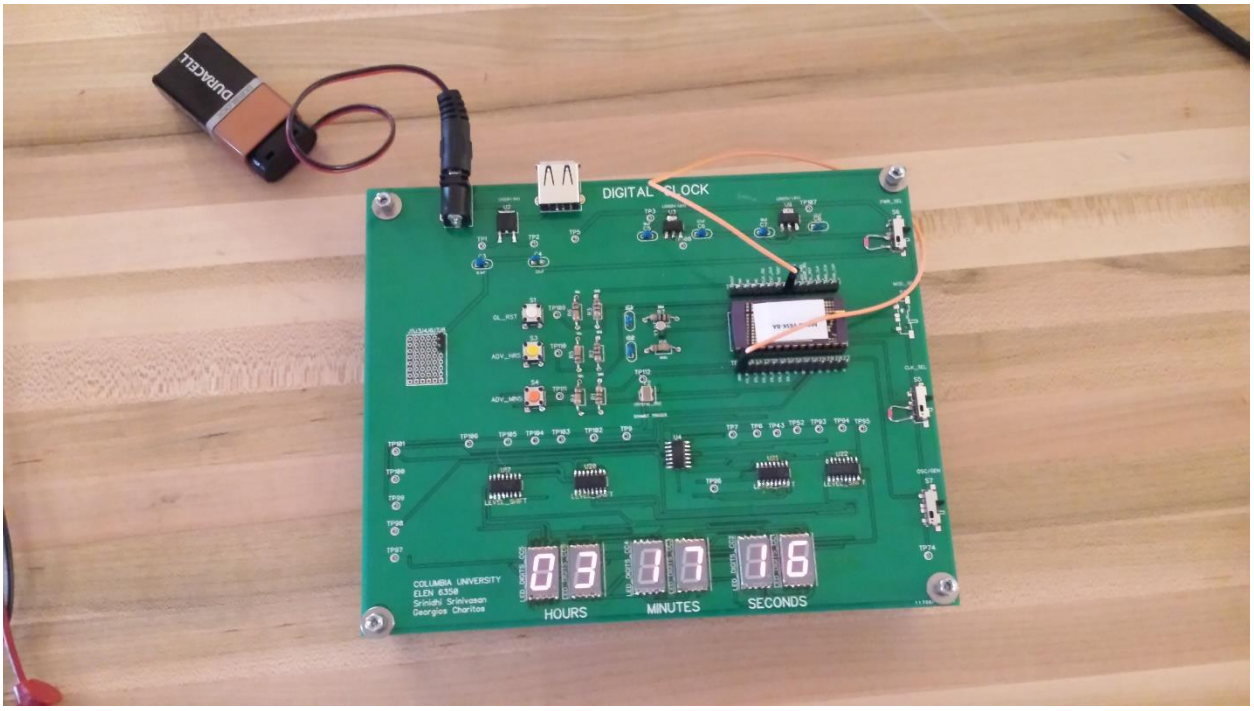


Fig. 5.6: Final Product operation